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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,834	08/30/2000	Joseph Link	TESSERA 3.0-132 DIV	2748

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EXAMINER

GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/650,834

Applicant(s)

LINK, JOSEPH

Examiner

David E Graybill

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 August 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3. 6) ☐ Other: _____

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Claim 17 is objected to because the claim has no end punctuation.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-6, 8-12, 14 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ramos (6119927).

At column 5, line 16 to column 6, line 47, Ramos teaches the following:

1. A stencil assembly for placing conductive elements over conductive pads provided at a first surface of a microelectronic element, said stencil assembly comprising: a main body 30 having a top surface and a bottom surface and a plurality of openings 31 extending between the top and bottom surfaces, said main body being adapted for overlying the first surface of said microelectronic element so that said openings are in substantial alignment with the pads accessible thereat; and a spacer element

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20 under the bottom surface of said main body, said spacer element being adapted for maintaining said main body above the first surface of said microelectronic element and remote from said pads.

2. The stencil assembly as in 1, wherein said spacer element is attached to the bottom surface of said main body.

3. The stencil assembly as in 2, wherein said spacer element includes one or more ribs (cavity walls) extending along the bottom surface of said main body.

4. The stencil assembly as in 3, wherein said ribs are integrally connected to and project from the bottom surface of said main body.

5. The stencil assembly as in 1, wherein said spacer element includes a substantially flat plate adapted for lying between the bottom surface of the main body and a first surface of a microelectronic element.

6. The stencil assembly as in 5, wherein the substantially flat plate of said spacer element includes one or more openings extending therethrough.

8. The stencil assembly as in 1, wherein said main body includes a substantially flat plate.

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9. The stencil assembly as in 8, wherein said substantially flat plate of said main body has a thickness of approximately 160-200 microns.

10. The stencil assembly as in 1, further comprising a reservoir 37 disposed over the top surface of said main body, said reservoir being adapted to retain said conductive elements remaining over the top surface of said main body after conductive elements have been deposited in the plurality of openings extending between the top and bottom surfaces of said main body.

11. The stencil assembly as in 10, wherein said reservoir includes a central aperture extending therethrough, said central aperture defining side walls adapted for retaining said conductive elements over the top surface of said main body.

12. The stencil assembly as in 1, wherein said microelectronic element includes a dielectric substrate 69.

14. An assembly comprising: a microelectronic element 23 having a first surface and one or more terminals 61 accessible at said first surface; a spacer plate having a top surface, a bottom surface and at least one opening extended therethrough secured over the first surface of said microelectronic element, wherein said at least one opening of said spacer plate is in substantial alignment with said terminals; a stencil having a top surface

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and a bottom surface and a plurality of openings extending therethrough secured over said spacer plate so that the plurality of openings in said stencil are in substantial alignment with said terminals, wherein said spacer plate holds said stencil remote from said terminals, and wherein conductive elements are deposited through the openings in said stencil so that each said deposited conductive element is affixed atop one of said terminals.

16. The assembly as in 14, wherein said spacer plate includes a substantially flat plate that is disposed between the first surface of said microelectronic element and the bottom surface of said element stencil.

17. The assembly as in 14, wherein said stencil has a thickness of approximately 160-200 microns.

18. An assembly comprising: a microelectronic element having a first surface and one or more terminals on said first surface, wherein a mass of flux material is deposited over each said terminal; a spacer plate having a top surface, a bottom surface and at least one opening extending therethrough over the first surface of said microelectronic element so that said at least one opening is in substantial alignment with said terminals; a stencil including a substantially flat plate having a top surface and a bottom surface and a plurality of openings

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extending between the top and bottom surfaces being secured over said spacer plate so that the plurality of said openings extending between the top and bottom surfaces being secured over said spacer plate so that the plurality of said openings in said stencil are in substantial alignment with said masses of flux material; and a conductive element being deposited in each said opening in said stencil, wherein each said deposited conductive element is positioned atop one of said masses of flux material.

To further clarify the teaching wherein said substantially flat plate of said main body has a thickness of approximately 160-200 microns, as cited, Ramos teaches that a thickness of the plate is "approximately two times the solder ball diameter," and the solder ball diameter is "0.005-0.035 inches." Therefore, a thickness of the plate is equal to 160-200 microns.

To further clarify the teachings wherein a mass of flux material is deposited over each said terminal, the plurality of said openings in said stencil are in substantial alignment with said masses of flux material, and each said deposited conductive element is positioned atop one of said masses of flux material, it is noted that claim 11 further limits the scope of claim 1 to an embodiment wherein a mass of flux material is not deposited over the terminals, the plurality of openings in the stencil are not in substantial alignment with masses of flux material, and

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each deposited conductive element is not positioned atop one of the masses of flux material. Therefore, it is inherent that the scope of claim 1 includes wherein a mass of flux material is deposited over the terminals, the plurality of openings in the stencil are in substantial alignment with masses of flux material, and each deposited conductive element is positioned atop one of the masses of flux material.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramos (6119927).

As cited, Ramos teaches the following:

7. The stencil assembly as in 1, wherein the top surface of said stencil and the first surface of said microelectronic element define a distance that is relative to the diameter of said conductive elements, so that said conductive elements do not substantially protrude over the top surface of said stencil when said conductive elements are over said pads.

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15. The assembly as in 14, wherein the top surface of said conductive element stencil and the first surface of said microelectronic element define a distance that is relative to the diameter of said conductive element so that said conductive elements do not substantially protrude over the top surface of said conductive element stencil when said conductive element stencil is positioned atop the first surface of said microelectronic element.

However, Ramos does not appear to explicitly teach wherein the top surface of said stencil and the first surface of said microelectronic element define a distance that is approximately equal to the diameter of said conductive elements.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular dimension because applicant has not disclosed that the dimensions is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the product would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are

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otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramos as applied to claim 1, and further in combination with Le Coz (5762258).

Ramos does not appear to explicitly teach the following:
13. The stencil assembly as in 1, wherein said microelectronic element includes a printed circuit board.

Regardless, in the abstract, Le Coz teaches wherein a microelectronic element includes a printed circuit board. Furthermore, it would have been obvious to combine the product of Le Coz with the product of Ramos because it would advantageously provide a microelectronic element.

Claim 18 is rejected in the alternative under 35 U.S.C. 103(a) as being unpatentable over the combination of Ramos (6119927) and Gordon (5934545).

As cited supra, Ramos teaches the following:
18. An assembly comprising: a microelectronic element having a first surface and one or more terminals on said first surface; a

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spacer plate having a top surface, a bottom surface and at least one opening extending therethrough over the first surface of said microelectronic element so that said at least one opening is in substantial alignment with said terminals; a stencil including a substantially flat plate having a top surface and a bottom surface and a plurality of openings extending between the top and bottom surfaces being secured over said spacer plate so that the plurality of said openings extending between the top and bottom surfaces being secured over said spacer plate so that the plurality of said openings in said stencil are in substantial alignment with said terminals; and a conductive element being deposited in each said opening in said stencil, wherein each said deposited conductive element is positioned atop one of said terminals.

However, because Ramos does not appear to explicitly teach wherein a mass of flux material is deposited over each said terminal, the plurality of said openings in said stencil are in substantial alignment with said masses of flux material, and each said deposited conductive element is positioned atop one of said masses of flux material, Ramos is rejected in the alternative in combination with Gordon.

Specifically, at column 5, lines 26-30, and column 5, line 60 to column 6, line 33, Gordon teaches wherein a mass of flux

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material is deposited over terminals 12, a plurality of openings in a stencil 24 are in substantial alignment with the masses of flux material, and each deposited conductive element 34 is positioned atop one of the masses of flux material. Moreover, it would have been obvious to combine the product of Gordon with the product of Ramos because it would facilitate conductive element attachment.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.



David E. Graybill
Primary Examiner
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D.G.
4-Sep-02

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